

Personal Information

Date of birth: December 11th, 1977
Country of citizenship: Italy
Permanent address: Via Rettore Calzone n. 27, 08020 Gavoi (NU), Italy
Mobile phone: (+39) 3285943689
Personal e-mail: marco@pypeople.com
IdonApple e-mail: marco.buttu@idonapple.com
Skype contact: marco-buttu
Home URL: www.pypeople.com

Education

Master of Science in Electronic Engineering, Università degli Studi di Cagliari, Cagliari, Italy, March 2007. Dissertation title: *Design of low power dissipation Network on Chip architectures (Sviluppo di architetture VLSI a bassa dissipazione di potenza per Network on Chip)*¹. Final grade: 110/110 summa cum laude.

High School Diploma, Istituto Tecnico per Geometri “Carmelo Floris”, Gavoi, Nuoro, Italy (September 1991 - July 1996). Final grade: 60/60.

Employment History

IdonApple Software Factory Gavoi (Sardinia, Italy)
Founder member March 2008 – Currently
I am founder member of IdonApple Software Factory, a young and dynamic team of engineers and programmers. My topics are *database-oriented* web applications development (either custom or standalone), GUI development, management and planning activities. I mainly develop using Python as a programming language and Django as a web framework.

National Institute for Astrophysics Capoterra (Sardinia, Italy)
Researcher December 2008 – Currently
Currently I am also Software Engineer for Italian National Institute for Astrophysics, for which I am writing the control software of SRT (Sardinia Radio Telescope, a 64 meter parabolic antenna) and Medicina (Bologna, Italy) radiotelescope (a 32 meter parabolic antenna). I use the C++ programming language to write low level components and Python to write GUI and everything else.

¹www.pypeople.com/mediafiles/papers/stuffs/thesis_book.pdf

Università degli Studi di Cagliari
Ecole Polytechnique Fédérale de Lausanne

Cagliari (Italy), Lausanne (Switzerland)

Researcher

April 2007 – January 2008

I worked on the topics of middleware and software for multiprocessor systems on chip at the University of Cagliari and at the Ecole Polytechnique Fédérale de Lausanne. In particular my research activity concerned thermal balancing policies based on task migration.

Activities and work tools:

- + I developed thermal balancing algorithms (based on task migration) for embedded multiprocessor systems on chip by using the C language. The algorithms was ported on a FPGA-based hardware emulation infrastructure on which each processor runs its own instance of the uClinux OS (Linux embedded) in the private memory.
- + Research activity about thermal balancing policies on which have benchmark. The results of this work was been published in *Thermal Balancing Policy for Streaming Computing on Multiprocessor Architectures*.
 - C programming language: it was used to write thermal balancing algorithms.
 - Python language : it was used to process simulation output files and for scripting.
 - Embedded Development Kit: hardware/software tool used to develop.
 - XUP Virtex-II Pro: board on which the hardware/software was emulated.
 - ViM, OpenOffice Spreadsheet, L^AT_EX: they were used to edit files, to make plot and to write documents.
 - Subversion: it was used to manage software version.

Università degli Studi di Bologna,
Dip. di Elettronica, Informatica e Sistemistica

Bologna, Italy

Freelance

October 2005 – March 2006

Research activity about Network on Chip in the SRC-Penn State University project. The activity of collaboration concerned the design in Verilog RTL of several \times pipes Network on Chip components, the \times pipes frequency and power optimization, and the development of automated design flow for low power Network on Chip.

Activities and work tools:

- + High-speed buffered crossbar switch design using Verilog RTL language for \times pipes NoC.
- + \times pipes NoC frequency and power optimization.
- + Development of low power automated design flow for Network on Chip.
 - Verilog language: it was used to design the RTL switch.
 - Python language: it was used to develop a GUI program (*xpySwitch*) on which make a particular instance of RTL switch.
 - ModelSim: it was used to edit Verilog code, to debug, to RTL and post-synthesis and post-layout simulation.
 - Synopsys Design Compiler, Prime Power e Design Vision: they were used to synthesize.
 - Cadence SoC Encounter: it was used to make the layout.
 - L^AT_EX, OpenOffice Draw e Spreadsheet: they were used to write the documents.
 - ViM e Subversion: they were used to edit the files and to manage software version.

Publications

Conference papers:

- Fabrizio Mulas, Marco Buttu, Michele Pittau, Salvatore Carta, David Atienza, Andrea Acquaviva, Luca Benini, and Giovanni De Micheli, *Thermal Balancing Policy for Streaming Computing on Multiprocessor Architectures*, in Design, Automation and Test in Europe (DATE '08), no. ISSN: 1530-1591/05, (Munich. Germany), 2008.

Computer Skills

Operating systems: Unix/Linux, Windows XP/2000/NT/98/95.

Markup and style languages: L^AT_EX, XHTML, RestructuredText, CSS.

Editing tools: ViM, Adobe PhotoShop, Gimp, OpenOffice.

Programming languages: Python, C/C++.

Web frameworks: Django.

Hardware description languages: Verilog.

Hardware design tools:

- *Synopsys*: Design Compiler, Prime Power, Design Vision;
- *Cadence*: SoC Encounter;
- *Xilinx*: Embedded Development Kit (EDK), Integrated Software Environment (ISE);
- *ModelTech*: ModelSim.

Foreign Languages

Italian: mother tongue.

English: speak: elementary; read: good; write: low-intermediate.

French: speak: low-intermediate, read: good; write: elementary.